REMARKS/ARGUMENTS

Claims 1-21 and 29-32 are pending.

A restriction requirement was imposed by the examiner in a telephone conversation held on February 2, 2005. The undersigned affirms claims 22-28 are withdrawn from examination without prejudice in response to the restriction requirement, and that claims 1-21 and 29-32 are elected for examination. The undersigned is authorized to make this election by way of a Power of Attorney filed December 11, 2000.

Claims 1, 7, 14, 15, 18-21, and 30-32 are rejected under 35 U.S.C. § 102(b) as being unpatentable by Koto et al., U.S. Patent No. 6,671,376.

Claims 2-6, and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Koto et al., U.S. Patent No. 6,671,376 in view of Fujinami et al., U.S. Patent No. 6,192,189.

Claims 8-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Koto in view of Copeland et al., U.S. Patent No. 5,659,613.

Claims 16 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Koto et al. in view of Yamagata et al., U.S. Patent No. 5,956,460.

Claim 29 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Koto et al. in view of Hashimoto, U.S. Patent No. 6,826,289.

The present invention as recited in claim 1 sets forth an apparatus for playing back data stored on an optical disk to produce data that is to be played back. The apparatus includes "a reproduction processing circuit" configured to produce the data. A subset of the data is stored in "a data store." A "detecting circuit" produces a detection result based on a watermark contained in the stored subset. A "control circuit" selectively outputs the data based on the detection result.

Koto et al. Does Not Teach "a reproduction processing circuit"

Koto et al. was cited for showing these aspects of the present invention. Fig. 1 of Koto et al. was cited for showing "a reproduction processing circuit." Fig. 1 of Koto et al. shows a video coding system 100A and a video decoding system 200A. It is not clear in the Office

action details whether all of Fig. 1 or a component shown in Fig. 1 was cited for showing "a reproduction processing circuit." Based on the understanding of one of ordinary skill, Applicant believes that the examiner must have intended the video decoding system 200A to be "a reproduction processing circuit" since the video coding system 100A does not reproduce, but rather creates the video data to be reproduced.

The video decoding system 200A in Fig. 1 of Koto et al. shows:

(1) coded video data from the video encoder 108 is output to transmission line 120;

(2) the coded video data on the transmission line 120 enters the decoder 201;

(3) the 2nd digital watermark detector 203 detects scramble key information 212 according to a video signal 211 decoded by the decoder 201;

(4) the video signal 211, scramble key information 212, and externally input second information 213 are sent to the descrambler 202 to obtain a descrambled video signal 214; and

(5) the descrambled video signal 214 is output as output signal 215.

The reproduction process of Fig. 1, therefore, refers to a process in which coded video data on a transmission line is decoded and then descrambled using scramble key information 212 detected by the 2nd digital watermark detector to output the descrambled video signal 214 as an output signal 215.

By comparison, the reproduction process circuit of the present invention includes a reproduction processing circuit, shown by example as block 14 in Fig. 1 of the instant application. This block performs reproduction processing of first data e.g., visual and audio information from an information recording medium and second data contained in the first data as additional data for the first data, and performs digital signal processing. The processing includes rearranging data in accordance with the format in which the reproduction signal is recorded and correcting errors. In addition, as can be seen from the example embodiment shown in Fig. 1, the block 14 receives a signal which has been detected from the optical disk 11 using the pickup 12

and amplified to a prescribed signal level by the preamplifier 13. Demodulation is thus performed in accordance with data read from an information recording medium such as the optical disk 11. Therefore, the reproduction process in this present invention refers to digital signal processing for reproduction of first data from an optical disk information recording medium including rearranging data in accordance with the format in which the reproduction signal is recorded and correcting errors, namely a process of demodulating a signal recorded on an optical disk. It is earnestly submitted that the reproduction processing circuit of the present invention is clearly different from the reproduction processing circuit taught by Koto et al. in terms of configuration and functionality, and that the Section 102 rejection of the claims is believed to be overcome.

Koto et al. Does Not Teach "a data store configured to receive a subset of the data"

Fig. 7 of Koto et al. was cited for showing "a data store configured to receive a subset of the data," and in particular, the RAM 38 was cited. The RAM 38 is a component of the scrambler 103 shown in Figs. l, 2, and 5. According to Fig. l, the digital watermark multiplexer 101 multiplexes a video signal 111 and a digital watermark signal 112 and outputs the multiplexed signal. Referring to Fig. 7, the scrambler 103 receives the multiplexed signal. The signal enters the scrambler 103 and is divided into a sync signal 45 and a signal 46 by the demultiplexer 37 (Fig. 7). The signal 46 is stored in the RAM 38 temporarily. As mentioned above, the data stored in the RAM 38 is the video signal 111 multiplexed with the digital watermark signal 112. The data stored in the RAM 38 is output according to readout address 47 output from the address generator 36. Although there is no mention of write address which is output from the address generator 36 for recording into the RAM 38, it is stated on column 13 line 59 and subsequent lines that in recording and reproduction with the RAM 38, a scramble process is performed where input data into the RAM 38 and output data from it are rearranged by changing the order of address data from the address generator 36. This clearly demonstrates that a set of addresses appearing on 47 for writing to the RAM 38 is different from that for reading from it. Accordingly, it can be said that the RAM 38 is intended to scramble the signal 46 which results from multiplexing of the video signal 111 and the digital watermark signal 112.

On the other hand, as shown in the illustrative embodiment according to the present invention, the data store (buffer memory 23) is intended to ensure proper operation of the watermark detection block 17 by temporarily storing reproduction data 24 output from the reproduction signal processing block 14 at high speed through the data buffer control block 16 and outputting it at a speed appropriate to the watermark detection block 17, as described in Fig. 1 and on page 8 lines 15-33 of the instant specification. The usage of the buffer memory 23 is described in more detail in Figs. 2-6 and on page 9 line 26 through page 11 line 14. From this, it can be said that this application uses the buffer memory 23 to absorb the difference in processing speed between the reproduction signal processing block 14 and the watermark detection block 17 and enables these two blocks to operate at their respective prescribed speeds and function in conj unction with each other.

From the above explanation, it is apparent that the RAM 38 as a data store taught by Koto et al. is completely different from the buffer memory 23 as a data store in this application in its position in the system where it is incorporated, the type of data which it stores, and its usage as a data store and its purpose. For at least this reason, the Section 102 rejection of the claims is believed to be overcome.

Koto et al. Does Not Teach "a detecting circuit"

Fig. 7 was further cited for showing "a detecting circuit" as recited in the pending claims. In particular, the address generator was asserted to show "a detecting circuit." As understood, the address generator 36 in Fig. 7 is intended to output an address for reading data stored in the RAM 38 and not to detect memory input or output. This seems clear from the fact that the information used to generate an address from the address generator 36 are seed 41 and sync signal 145. More significantly, either the signal 46 input in the RAM 38 nor the scrambled video signal 44 output from the RAM 38 are used.

The examiner argues that it is suggested on column 14 lines 8-23 that the address generator 36 generates a readout address and thus detects memory input and output; however, there is no such description. On the contrary, the cited lines simply state that:

> "An address generator 36 generates the readout address 47 of the picture memory 38 on the basis of the scramble pattern from the scramble pattern generator 35, thus reading out picture data. The descramble key generated by the descramble key generator 32 is coded by a key encoder 33, and is output as the descramble key 43." *(underlining added to highlight)*

It is earnestly submitted that there is no "detection" of the input and output of memory. There is only generation of a readout address. Furthermore, there is no detection result based on a watermark.

By comparison, in the present invention, the watermark detection process 17 described on page 6 lines 9-12 is connected via the data buffer controller 16 to the buffer memory 23 so that the watermark detection process 17 processes data stored in the buffer memory 23 to obtain the result of watermark detection. The detection result is at least based on the second data (namely watermark) contained in the data stored in the buffer memory 23.

Based on the above explanation, it is respectfully and earnestly submitted that the examiner appears to have misinterpreted the system by Koto et al. by asserting that the address generator 36 detects memory input/output on the grounds that it generates an address. Comparing to the present invention, the detection of a watermark as second data is made from the first data stored in the memory; the detection of the watermark bears no relation to memory address generation.

For at least this reason, the Section 102 rejection of the claims is believed to be overcome.

Koto et al. Does Not Teach "a control circuit"

Fig. 7 was further cited for showing "a control circuit" as recited in the pending claims. The examiner asserted that the address generator 36 selects the output from the memory to be outputted into the system, citing column 14, lines 8-43.

As explained above, the address generator 36 does not detect memory content and thus does not output first data selectively on the basis of any detection result. In addition, column 14, lines 8-43 included not only a description of Fig. 7 but also a description of Fig. 8. Figure 8 is a variation of Fig. 7 and the matters disclosed in both the figures are not different in

essence. Therefore, the cited lines do not describe that first data is selectively output on the basis of the result of detection by the control circuit.

On the other hand, in the present invention as illustrated by the embodiment in Fig. 1 and described on page 6 lines 18-24 and page 7 lines 4-14, data output from the reproduction signal output control process 15 is controlled according to the detection result which is sent from the watermark detection process 17 to the system control process 19 via the exclusive data bus 25. Specifically, output from the signal output terminal 18 is controlled according to copy control, as described on page 6 lines 25-31.

From the above explanation, it is earnestly submitted that there was a misinterpretation in the system by Koto et al. in the assertion the address generator 36 selects data which is output from the memory to the system. In the present invention, the detection result from the watermark detection operation is introduced into the system control process 19; the system control process 19 controls a signal which is sent from the reproduction signal output control process 15 to the signal output terminal 18.

For at least this reason, the Section 102 rejection of the claims is believed to be overcome.

Section 102 Rejection of Claim 7 is Overcome

The data bus recited in pending claim 7 was asserted to be shown in Fig. 7 of Koto et al. The examiner asserted that in the system by Koto et al, Fig. 7 shows that the detection circuit 35 and the control circuit 36 are connected via a data bus to the data store 38. Most respectfully, however, this is a misinterpretation. In Fig. 7, the pattern generator 35 functions to generate a scramble pattern based on output of the second random number generator 34, but has no function of signal detection. Further, the address generator 36 functions to generate address data for the RAM 38 according to a signal from the pattern generator 35, but has no function to control an object upon according to a signal from the pattern generator 35. Both 35 and 36 are not configured to be connected to the RAM 38 via the data bus.

For any of the foregoing reasons, the Section 102 rejection of claim 7 is believed to be overcome.

Section 102 Rejection of Claims 14 and 15 is Overcome

On column 14 line 59 and subsequent lines in the cited reference, operation of the multiplexer 54 of Koto et al. is explained. The multiplexer 54 multiplexes a coded signal 63 and a coded signal 64 and outputs the multiplexed data as scrambled coded data 49. On the other hand, claim 14 of the present invention recites an additional aspect of the present invention in which the data store receives at least some of the data at a data rate equal to a data rate at which the reproduction processing circuit produces the data. See also claim 15. Respectfully, it seems that the examiner's explanation is based on a misreading of the present invention as recited in claim 14 because the cited reference includes no reference to a data rate and also no reference to data reception by the RAM 51 which is presumed to have a data store function. The rejection of claims 14 and 15 is therefore believed to be overcome for any one of the foregoing reasons.

Section 102 Rejection of Claim 19 is Overcome

Although the examiner states that Fig. 1 of Koto et al. shows data input through the input means 111, it is mentioned on column 9 line 61 that 111 is a video signal. On the other hand, in present invention, a data source denotes a reproduction signal process 14 and data 24 received from it is general digital data obtained by demodulating a signal stored on an optical disk by the reproduction signal process 14 and is not limited to a video signal.

Although the examiner states that Fig. 7 in the cited reference shows the result of detection by the pattern generator and address generator which is data processed as described on column 14 lines 9-36, the input signal for the pattern generator and the address generator is originally the seed 41 and the sync signal 45. The sync signal 45 is a signal demultiplexed from the video signal 42 by the demultiplexer 37. Here, the seed 41 and the sync signal 45 are not stored in the RAM 38 and, in this sense, the input signal for the pattern generator and address generator is not a signal which is stored in the RA 38. Therefore, detected data is not detected from the data stored in the RAM- 38. On the other hand, in this application, data which undergoes watermark detection is data which is once stored in the buffer memory 23, then read from the buffer memory 23 and in this sense, detection result is obtained by processing data in the data store. Besides, while this application describes that the detection result is based on a

watermark, it is clear that in the cited reference the result of detection by the pattern generator and the address generator is not based on a watermark because the pattern generator and the address generator have no function to detect a watermark.

Although the examiner states that column 14 lines 36-43 in the cited reference implies selective output based on the detection result, the cited lines explain that the sync signal 61 which is output from VLD 52 based on data stored in the RAM 38 is sent to the scramble pattern generator 30B and data is output from the RAM 51 according to the readout address 47 output from the scramble pattern generator 30B. In other words, the detection result on which selective data output is based is obtained when the sync signal 61 from VLD 52 is added to the scramble pattern generator 30B. Since VLD 52 and the scramble pattern generator 30B have no watermark detection function, it is apparent that the detection result on which selective data output is based is not based on any watermark. On the other hand, in this application, the detection result on which selective data output is based is based on a watermark.

For any one of the foregoing reasons, it is earnestly submitted that the Section 102 rejection of claim 19 is overcome.

Section 103 Rejection of the Claims

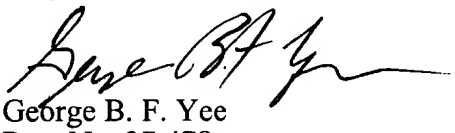
The Section 103 rejection of the dependent claims are believed to be overcome on the basis that their respective base claims are not taught by Koto et al. and are thus patentably distinct over Koto et al.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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